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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,279	02/15/2006	Gordon John Allan	51959-1 /slr	3290

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
09/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/568,279	ALLAN, GORDON JOHN	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-32* is/are allowed.

6)☒ Claim(s) *33-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/15/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 33-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (JP 55052596).

As to claim 33, Tanaka's figure 4, 5 and 7 show a circuit comprising: at least one control input (Φ) defining at least a first control state and a second control state; a plurality of mixed-signal outputs (outputs of 20n) each characterized by a respective on state (high), a respective off state (low), and a respective analog range (tri-state); a set of circuit elements (20n) connected to cause sequential transitions of any mixed-signal output that is in a respective off state or in the respective analog range towards a respective on state during a first control state (when IN is high), and to cause sequential transitions of any mixed-signal output that is in a respective on state or in the respective analog range towards a respective off state during a second control state (when IN is low).

As to claim 34, figures 4, 5 and 7 show that the on states are all logic high and the off states are all logic low.

As to claim 35, figures 4, 5 and 7 show that the on states alternate between being logic high and logic low, and the off states alternate between being logic low and logic high.

3. Claims 36-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (USP 6515648).

As to claim 36, Tanaka et al.'s figure 2 shows a method for dynamically determining if a particular output of a set of mixed-signal outputs (output of 2n1) representing a mixed signal code is outputting an analog value, the method comprising: receiving (by 2n2) at least one neighboring mixed-signal outputs (2n1); determining if the neighboring mixed-signal outputs are consistent with the particular mixed-signal output being an analog value (tri-state) for the mixed-signal code (the output of 2n2 is unchanged when 2n1 is in tri-state).

As to claim 37, figure 2 shows that the mixed-signal code is a thermometer code (may be any value).

As to claim 38, figure 2 shows the step of dynamically connecting at least one additional capacitance (3n0) or filter stage to the mixed-signal outputs that are outputting analog values.

As to claim 39, figure 2 shows the step of maintaining (tri-state) a respective state for each of the mixed-signal outputs that are outputting analog values.

As to claim 40, figure 2 shows a method for processing a set of mixed-signal outputs, the method comprising: detecting (by 2n2) when a particular mixed-signal output has reached a digital state (when 2n2 changes its state); upon detecting that a particular mixed-signal output has reached a digital state, securing the particular mixed-signal output to an appropriate reference (by buffers 3n0 and 3n1).

As to claim 41, figure 2 shows that the set of mixed-signal outputs represent a mixed-signal code, and wherein detecting when a particular mixed-signal output has reached a digital state comprises: receiving at least one neighboring mixed-signal outputs (output of 2n1); determining if the neighboring mixed-signal outputs are consistent with the particular mixed-signal output being a digital state for the mixed-signal code.

Allowable Subject Matter

4. Claims 1-32 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

August 30, 2007